Amendments to the Claims

Please amend the claims as indicated in the list of claims provided below:

1. (Original): Data processing apparatus comprising:

(i) a processor core operable to execute successive program instruction words of a predetermined plurality of instruction sets stored in a data memory;

(ii) a program counter register for indicating an address of a next program instruction word in said data memory;

(iii) logic operable to modify the contents of said program counter register in response to a current program instruction word;

(iv) a processor core controller, responsive to one or more predetermined indicator bits of said program counter register, operable to control said processor core to execute program instruction words of a current instruction set selected from said predetermined plurality of instruction sets and specified by the state of said one or more indicator bits of said program counter register; and

(v) a memory access controller operable to access program instruction words stored in said data memory, said access controller not being responsive to said one or more indicator bits of said program counter register.

2. (Original): Apparatus according to claim 1, comprising:

a first instruction decoder for decoding program instruction words of a first instruction set; and

a second instruction decoder for decoding program instruction words of a second instruction set;

and in which said processor core controller is operable to control either said first instruction decoder or said second instruction decoder to decode a current program instruction word.

3. (Original): Apparatus according to claim 2, in which:

program instruction words of said first instruction set are X-bit program instruction words; and

program instruction words of said second instruction set are Y-bit program instruction words;

Y being different to X.

4. (Original): Apparatus according to claim 1, in which:

program instruction words of a first instruction set are X-bit program instruction words; and

program instruction words of a second instruction set are Y-bit program instruction words;

Y being different to X.

5. (Original): Apparatus according to claim 3, in which Y is 16 and X is 32.

6. (Original): Apparatus according to claim 4, in which Y is 16 and X is 32.

7. (Original): Apparatus according to claim 1, in which said one or more indicator bits of said program counter register are one or more most significant bits of said program counter register.

8. (Original): Apparatus according to claim 1, in which said one or more indicator bits of said program counter register are one or more least significant bits of said program counter register.

9. (Original): Apparatus according to claim 2, in which said one or more indicator bits of said program counter register are one or more least significant bits of said program counter register.

10. (Original): Apparatus according to claim 3, in which said one or more indicator bits of said program counter register are one or more least significant bits of said program counter register.

11. (Original): Apparatus according to claim 4, in which said one or more indicator bits of said program counter register are one or more least significant bits of said program counter register.

12. (Original): Apparatus according to claim 5, in which said one or more indicator bits of said program counter register are one or more least significant bits of said program counter register.

13. (Original): Apparatus according to claim 6, in which said one or more indicator bits of said program counter register are one or more least significant bits of said program counter register.

14. (Original): Apparatus according to claim 1, comprising a data memory for storing program instruction words to be executed.

15. (Original): A method of switching between a predetermined plurality of instruction sets used by a data processing apparatus, the method comprising:

in response to a first instruction:

(i) accessing a sequence of bits, the sequence of bits having an address portion and an instruction set indicator portion;

(ii) identifying an instruction set selected from the predetermined plurality of instruction sets based on the instruction set indicator portion of the sequence of bits;

(iii) setting one or more control flags to indicate that a current instruction set for the data processing apparatus is the instruction set identified based on the instruction set indicator portion of the sequence of bits; and

retrieving a second instruction from an address derived from the address portion of the sequence of bits,

wherein the instruction set identified by the instruction set indicator portion of the sequence of bits is identifiable without regard to the address derived from the address portion of the sequence of bits.

16. (Original): The method of claim 15, further comprising executing the second instruction as an instruction of the current instruction set.

17. (Original): The method of claim 15 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein

instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X.

18. (Original): The method of claim 17 wherein X is 32 and Y is 16.

19. (Original): The method of claim 15 wherein the instruction set indicator portion of the sequence of bits comprises one or more least significant bits of the sequence of bits.

20. (Original): The method of claim 15 wherein the instruction set indicator portion of the sequence of bits comprises one or more most significant bits of the sequence of bits.

21. (Original): A method of switching between a predetermined plurality of instruction sets used by a data processing apparatus, the method comprising:

in response to a first instruction:

(i) accessing a sequence of bits, the sequence of bits having an address portion and an instruction set indicator portion, the instruction set indicator portion having at least one bit that is not part of the address portion of the sequence of bits;

(ii) identifying an instruction set selected from the predetermined plurality of instruction sets based on the instruction set indicator portion of the sequence of bits;

(iii) setting one or more control flags to indicate that a current instruction set for the data processing apparatus is the instruction set identified based on the instruction set indicator portion of the sequence of bits; and

retrieving a second instruction from an address derived from the address portion of the sequence of bits.

22. (Original): The method of claim 21, further comprising executing the second instruction as an instruction of the current instruction set.

23. (Original): The method of claim 21 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X.

24. (Original): The method of claim 23 wherein X is 32 and Y is 16.

25. (Original): The method of claim 21 wherein the instruction set indicator portion of the sequence of bits comprises one or more least significant bits of the sequence of bits.

26. (Original): The method of claim 21 wherein the instruction set indicator portion of the sequence of bits comprises one or more most significant bits of the sequence of bits.

27. (Original): A data processing apparatus capable of operating using instructions from a predetermined plurality of instruction sets, the data processing apparatus comprising:

(i) a processor core responsive to a first instruction to access a sequence of bits, the sequence of bits having an address portion and an instruction set indicator portion, the processor core deriving an address of a second instruction from the address portion of the sequence of bits and using the instruction set indicator portion of the sequence of bits to set one or more control flags; and

(ii) a controller responsive to the one or more control flags, the state of the one or more control flags specifying a current instruction set selected from the predetermined plurality of instruction sets, to cause the processor core to execute the second instruction as an instruction from the current instruction set,

wherein the one or more control flags are set without regard to the address derived from the address portion of the sequence of bits.

28. (Original): The apparatus of claim 27 wherein the one or more control flags comprise one or more predetermined bits in a program counter.

29. (Original): The apparatus of claim 27, further comprising a memory system, wherein the memory system is not responsive to the one or more control flags.

30. (Original): The apparatus of claim 27, further comprising a memory system wherein the one or more control flags are not provided to the memory system.

31. (Original): The apparatus of claim 27 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X.

32. (Original): The apparatus of claim 31 wherein X is 32 and Y is 16.

33. (Original): A data processing apparatus capable of operating using instructions from a predetermined plurality of instruction sets, the data processing apparatus comprising:

(i) a processor core responsive to a first instruction to access a sequence of bits to derive an address of a second instruction, the sequence of bits having an address portion and an instruction set indicator portion and the instruction set indicator portion having at least one bit that is not part of the address portion of the sequence of bits, the address of the second instruction being derived from the address portion of the sequence of bits;

(ii) the processor core using the instruction set indicator portion of the sequence of bits to set one or more control flags, the state of the one or more control flags specifying a current instruction set selected from the predetermined plurality of instruction sets; and

(iii) a controller responsive to the one or more control flags to cause the processor core to execute the second instruction as an instruction from the current instruction set.

34. (Original): The apparatus of claim 33 wherein the one or more control flags comprise one or more predetermined bits in a program counter.

35. (Original): The apparatus of claim 33, further comprising a memory system, wherein the memory system is not responsive to the one or more control flags.

36. (Original): The apparatus of claim 33, further comprising a memory system wherein the one or more control flags are not provided to the memory system.

37. (Original): The apparatus of claim 33 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X.

38. (Original): The apparatus of claim 37 wherein X is 32 and Y is 16.

39. (Original): A data processing architecture capable of operating using instructions from a predetermined plurality of instruction sets, the data processing architecture comprising:

(i) a processor core responsive to a first instruction to access a sequence of bits, the

sequence of bits having an address portion and an instruction set indicator portion, the processor core deriving an address of a second instruction from the address portion of the sequence of bits and using the instruction set indicator portion of the sequence of bits to set one or more control flags; and

(ii) a controller responsive to the one or more control flags, the state of the one or more control flags specifying a current instruction set selected from the predetermined plurality of instruction sets, to cause the processor core to execute the second instruction as an instruction from the current instruction set,

wherein the one or more control flags are set without regard to the address derived from the address portion of the sequence of bits.

40. (Original): The data processing architecture of claim 39 wherein the one or more control flags comprise one or more predetermined bits in a program counter.

41. (Original): The data processing architecture of claim 39, further comprising a memory system, wherein the memory system is not responsive to the one or more control flags.

42. (Original): The data processing architecture of claim 39, further comprising a memory system wherein the one or more control flags are not provided to the memory system.

43. (Original): The data processing architecture of claim 39 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X.

44. (Original): The data processing architecture of claim 43 wherein X is 32 and Y is 16.

45. (Original): A data processing architecture capable of operating using instructions from a predetermined plurality of instruction sets, the data processing architecture comprising:

(i) a processor core responsive to a first instruction to access a sequence of bits to derive an address of a second instruction, the sequence of bits having an address portion and an instruction set indicator portion and the instruction set indicator portion having at least one bit that is not part of the address portion of the sequence of bits, the address of the second

instruction being derived from the address portion of the sequence of bits;

(ii) the processor core using the instruction set indicator portion of the sequence of bits to set one or more control flags, the state of the one or more control flags specifying a current instruction set selected from the predetermined plurality of instruction sets; and

(iii) a controller responsive to the one or more control flags to cause the processor core to execute the second instruction as an instruction from the current instruction set.

46. (Original): The data processing architecture of claim 45 wherein the one or more control flags comprise one or more predetermined bits in a program counter.

47. (Original): The data processing architecture of claim 45, further comprising a memory system, wherein the memory system is not responsive to the one or more control flags.

48. (Original): The data processing architecture of claim 45, further comprising a memory system wherein the one or more control flags are not provided to the memory system.

49. (Original): The data processing architecture of claim 45 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X.

50. (Original): The data processing architecture of claim 49 wherein X is 32 and Y is 16.

51. (Original): A data processing apparatus capable of switching between a predetermined plurality of instruction sets, the data processing apparatus comprising:

(i) means for accessing a sequence of bits in response to a first instruction, the sequence of bits having an address portion and an instruction set indicator portion;

(ii) means for identifying an instruction set selected from the predetermined plurality of instruction sets based on the instruction set indicator portion of the sequence of bits in response to the first instruction;

(iii) means for setting one or more control flags to indicate that a current instruction set for the data processing apparatus is the instruction set identified based on the instruction set indicator portion of the sequence of bits in response to the first instruction; and

(iv) means for retrieving a second instruction from an address derived from the address

portion of the sequence of bits in response to the first instruction,

wherein the instruction set identified by the instruction set portion of the sequence of bits is identifiable without regard to the address derived from the address portion of the sequence of bits.

52. (Original): The data processing architecture of claim 51 wherein the one or more control flags comprise one or more predetermined bits in a program counter.

53. (Original): The data processing architecture of claim 51, further comprising a memory system, wherein the memory system is not responsive to the one or more control flags.

54. (Original): The data processing architecture of claim 51, further comprising a memory system wherein the one or more control flags are not provided to the memory system.

55. (Original): The data processing architecture of claim 51 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X.

56. (Original): The apparatus of claim 55 wherein X is 32 and Y is 16.

57. (Original): A method of operating a data processing apparatus, the method comprising:

(i) receiving a first instruction from a first instruction set selected from a predetermined plurality of instruction sets;

(ii) translating the first instruction to generate a first set of one or more control signals;

(iii) accessing a sequence of bits comprising an address portion and an instruction set indicator portion in response to the first set of one or more control signals, the instruction set indicator portion having at least one bit that is not part of the address portion of the sequence of bits;

(iv) setting one or more control flags based upon the value of the instruction set indicator portion of the sequence of bits to specify that a current instruction set is a second instruction set selected from a predetermined plurality of instruction sets;

(v) retrieving a second instruction using an address derived from the address portion of

the sequence of bits; and

(vi) translating the second instruction as an instruction from the current instruction set to generate a second set of one or more control signals.

58. (Original): The method of claim 57 wherein the predetermined plurality of instruction sets consists of two instruction sets.

59. (Original): The method of claim 57 wherein the first instruction set consists of X-bit instructions and the second instruction set consists of Y-bit instructions, Y being different from X.

60. (Original): The method of claim 58 wherein the first instruction set consists of X-bit instructions and the second instruction set consists of Y-bit instructions, Y being different from X.

61. (Original): The method of claim 59 wherein X is 32 and Y is 16.

62. (Original): The method of claim 60 wherein X is 32 and Y is 16.

63. (Original): The method of claim 59 wherein X is 16 and Y is 32.

64. (Original): The method of claim 60 wherein X is 16 and Y is 32.

65. (New): A program counter register comprising:

an ordered set of bits;

wherein a subset of the ordered set of bits identifies an address of an instruction; and at least one bit of the ordered set of bits identifies an instruction set; and

wherein the at least one bit is not a member of the subset.

66. (New): A method of selecting an instruction set comprising the steps of:

receiving a branching instruction written in a first instruction set of a plurality of instruction sets;

pursuant to the branching instruction, inserting the address of a next instruction into a register and setting the value of a flag, where the value of the flag is not dependent upon the address of the next instruction;

selecting an instruction set based upon the value of the flag; and

acquiring the next instruction at the address inserted into the register.

67. (New): A processing apparatus comprising:

a pointer for identifying an address of a next instruction that is written in a first instruction set of a plurality of instruction sets; and

a flag for identifying the first instruction set;

wherein:

the pointer and the flag are both written in response to an instruction from a second instruction set of the plurality of instruction sets, and

the value of the flag is not dependent upon the address of the next instruction.

68. (New): The apparatus of claim 67 wherein:

the first instruction set is different from the second instruction set.

69. (New): The apparatus of claim 67 wherein:

the pointer and the flag are located in a single register.

70. (New): The apparatus of claim 67 wherein:

the pointer and the flag are not located in a single register, yet are written to as if portions of a single register.